REMARKS

The Examiner is thanked for the thorough examination and search of the subject patent application and for finding patentable material in the claims. The Examiner is thanked for allowing claims 11-13, 15, 17, 19, 20, 23-25, 42-58, 60-62, 102-107, 109-111, 117-121, 123-126, 134-141, 143-161, 169-180 and 185-188.

Claims 11-13, 15, 17, 19-20, 23-25, 42-58, 60-71, 73, 74, 102-107, 109-111, 117-121, 123-129, 131-141, 143-188 are pending, wherein Claims 63 and 127 have been currently amended, and Claims 1-10, 14, 16, 18, 21-22, 26-41, 59, 72, 75-101, 108, 112-116, 122, 130 and 142 have been canceled.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 63, 65, 66, 68, 71 and 165-168

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As currently amended, independent claim 63 is recited below:

63. A method of fabricating an electronic package comprising the steps of:
joining a die, separated from a wafer, and a substrate, wherein an opening in said substrate exposes a topmost patterned circuit layer of said die; and
depositing a conductive material into said opening, wherein said conductive material is used to connect said topmost patterned circuit layer to an external circuitry.

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Reconsideration of Claims 63, 65, 66, 68, 71 and 165-168 rejected under 35 U.S.C. 103(a) as being unpatentable over Gaynes et al. (US 6,165,885) is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 63 patentably distinguishes over the citation by Gaynes et al. (US 6,165,885).

Gaynes et al. teach that a method for forming an electronic package comprises joining a wafer and a substrate. ~ *See Steps 100 and 120 in FIG. 1, lines 58-61, col. 10, line 66, col. 12 through line 2, col. 13, and lines 18-20, col. 16* ~ However, Gaynes et al. fail to teach, hint or suggest the step of joining a die, but not a wafer, and a substrate, which is claimed in claim 63.

The Examiner considers that "With respect to the limitation of joining the substrate with the die, while there no requirement in the claim that the die be separated one from another before joining with the substrate, it has been held that the selection of any order of process steps is prima facie obvious in the absence of new or unexpected results". ~ *See lines 1-4 in the last paragraph of page 2 in the last Office Action mailed Jun. 14, 2006* ~ Applicants respectfully traverse the Examiner's opinion. "Die" is typically well-known as a body separated from "Wafer". The wordings of "Die" and "Wafer" are unambiguous to those skilled in the art. The step of "joining a die and a substrate" claimed in Claim 63 means "joining a die, after it is separated from a wafer, and a substrate". The step of "joining a wafer and a substrate" taught by Gaynes et al means "joining a wafer, before separating it into multiple dies, and a substrate".

Applicants believe that those skilled in the art would not come up with the subject matter claimed in claim 63 because Gaynes et al. fails to teach the step of joining a die and a substrate, but teaches the step of joining a wafer and a substrate.

Furthermore, the limitation of "a die separated from a wafer" is added into claim 63. Therefore, the Examiner's concern that "the limitation is not in the claims" (~ *See line 6 in the first paragraph of page 6 in the last Office Action mailed Jun. 14, 2006* ~) should now be eliminated . Even if the limitation of "a die separated from a wafer" were not added into claim 63, those skilled in the art should understand that "a die is properly separated from a wafer".

Gaynes et al. teaches that "In step 128 the wafer is diced into a plurality of integrated computer chips. This step may be performed anywhere in the process of FIG. 1, but preferably done at the end to allow the entire wafer to be simultaneously processed in the method of the invention" ~ *See lines 46-50, col. 17* ~ Even though Gaynes et al. teaches that the step of dicing may be performed at any point in the process, Gaynes et al. fails to teach, hint or suggest the detailed packaging steps if the step of dicing the wafer is not performed at the end. There are so many choices to put step 128 between steps 100 and 102, steps 102 and 104, steps 104 and 106, steps 106 and 108, steps 108 and 110, steps 110 and 112, steps 112 and 114, steps 114 and 116, steps 116 and 118, steps 118 and 120, steps 120 and 122, steps 122 and 124, or steps 124 and 126. Based on Gaynes's vague disclosure, those skilled in the art should not immediately think of other possible steps if step 128 is not performed at the end. Applicants consider that the Gaynes et al's statement is of the type that gives only general guidance and is not at all specific as to the particular method of the claimed invention and how to achieve it. Such a suggestion

may make an approach "obvious to try" but it does not make the invention obvious. ~ *Id. at 1065 (citing In re O'Farrell, 853 F.2d 894, 7 USPQ 2d 1673, 1681 (Fed. Cir. 1988))* ~

For at least the foregoing reasons, applicants respectfully submit independent claim 63 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 64-71, 73-74 and 162-168 patently define over the prior art as well.

Response to Claims 127-129, 132, 133 and 181-184

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As currently amended, independent claim 127 is recited below:

127. A method of fabricating an electronic package comprising the steps of:
providing a die, separated from a wafer, comprising a pad and a passivation layer, an opening in said passivation layer exposing said pad; and
joining said die and a substrate, an opening in said substrate exposing said pad.

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Reconsideration of Claims 127-129, 132, 133 and 181-184 rejected under 35 U.S.C. 103(a) as being unpatentable over Gaynes et al. (US 6,165,885) is requested based on the following remarks.

Applicants respectfully assert that the method claimed in claim 127 patentably distinguishes over the citation by Gaynes et al. (US 6,165,885).

Gaynes et al. teach that a method for forming an electronic package comprises joining a wafer and a substrate. ~ *See Steps 100 and 120 in FIG. 1, lines 58-61, col. 10, line 66, col. 12 through line 2, col. 13, and lines 18-20, col. 16* ~ However, Gaynes et al. fail to teach, hint or suggest the step of joining a die, but not a wafer, and a substrate, which is claimed in claim 127.

The Examiner considers that "With respect to the limitation of joining the substrate with the die, while there no requirement in the claim that the die be separated one from another before joining with the substrate, it has been held that the selection of any order of process steps is prima facie obvious in the absence of new or unexpected results". ~ *See lines 1-4 in the third paragraph of page 3 in the last Office Action mailed Dec. 16, 2005* ~ Applicants respectfully traverse the Examiner's opinion. "Die" is typically well-known as a body separated from "Wafer". The wordings of "Die" and "Wafer" do not make those skilled in the art confused. The step of "joining a die and a substrate" claimed in Claim 63 means "joining a die, after separated from a wafer, and a substrate". The step of "joining a wafer and a substrate" taught by Gaynes et al means "joining a wafer, before separated into multiple dies, and a substrate". Applicants consider that those skilled in the art should not think up the subject matters claimed in claim 127 because Gaynes et al. fail to teach the step of joining a die and a substrate, but teach the step of joining a wafer and a substrate.

Furthermore, the limitation of "a die separated from a wafer" is added into claim 127. Therefore, the Examiner's concern that "the limitation is not in the claims" (~ *See line 6 in the first paragraph of page 6 in the last Office Action mailed Jun. 14, 2006* ~) should now be

eliminated. Even if the limitation of "a die separated from a wafer" were not added into claim 127, those skilled in the art should understand that "a die is properly separated from a wafer".

Gaynes et al. teach that "In step 128 the wafer is diced into a plurality of integrated computer chips. This step may be performed anywhere in the process of FIG. 1, but preferably done at the end to allow the entire wafer to be simultaneously processed in the method of the invention" ~ *See lines 46-50, col. 17* ~ Even though Gaynes et al. teach that the step of dicing may be performed at any point in the process, Gaynes et al. fail to teach, hint or suggest the detailed packaging steps if the step of dicing the wafer is not performed at the end. There are so many choices to put step 128 between steps 100 and 102, steps 102 and 104, steps 104 and 106, steps 106 and 108, steps 108 and 110, steps 110 and 112, steps 112 and 114, steps 114 and 116, steps 116 and 118, steps 118 and 120, steps 120 and 122, steps 122 and 124, or steps 124 and 126. Based on Gaynes's vague disclosure, those skilled in the art should not immediately think of other possible steps if step 128 is not performed at the end. Applicants consider that the Gaynes et al's statement is of the type that gives only general guidance and is not at all specific as to the particular method of the claimed invention and how to achieve it. Such a suggestion may make an approach "obvious to try" but it does not make the invention obvious. ~ *Id. at 1065 (citing In re O'Farrell, 853 F.2d 894, 7 USPQ 2d 1673, 1681 (Fed. Cir. 1988))* ~

For at least the foregoing reasons, applicants respectfully submit independent claim 127 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 128, 129, 131-133 and 181-184 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for Allowance, and that is so requested.

It is requested that should Examiner Owens not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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